REMARKS

Prior to amendment, Claims 15-24 and 27-44 were pending. After entry of the present amendment, Claims 15-20, 22-23 and 27-44 remain pending.

Response to Prior Amendment

In response to the prior amendment, the Examiner has withdrawn the rejections based upon Bai et al. in view of Elers et al. and Pomarade et al.

Present Amendments

To facilitate prosecution, Applicant has amended the two independent claims to recite particular gate electrode materials. Applicant submits that the amendments are fully supported by the application as filed. For example, please see original Claims 21 and 24, cancelled herewith.

Rejections

The Examiner has rejected the pending claims under 35 U.S.C. § 103(a) as being unpatentable over Bai et al. (U.S. Patent No. 6,166,417) in view of Matsuse et al. (U.S. Patent No. 6,861,356). Additional secondary references are employed to reject certain dependent claims.

As noted above, Applicant has amended Claims 15 and 42 to recite a particular list of electrode materials. Applicant submits that the amendment is fully supported, and furthermore that the list of materials lends greater context to the claims, as these are atypical gate electrode materials that are particularly useful for tuning work function with metallic gates at different regions of the substrate for CMOS processing.

The Examiner has withdrawn the prior rejections due to Applicant's amendments and arguments that obviated the Examiner's motivation for combining an ALD reference with Bai et al. Similarly, the present amendments emphasize a lack of motivation for the asserted combination, for the claims as amended.

In particular, Matsuse et al., like the previously asserted ALD references, do not teach a universally applicable motivation for using ALD for all diffusion barriers. The majority of the reference applies to barriers for damascene contexts, (Figures 1 and 2, 6A-6F) and within a gate stack between two conductive materials (e.g., Figure 3A, 9, 10B, 13A, 13B, etc.). Because

Applicant's claims are directed to depositing a barrier layer directly over the dielectric layer, the majority of this disclosure is not applicable.

Rather, the disclosure in Matsuse et al. regarding the usefulness of the ALD method for a barrier layer directly over a gate dielectric can be found in the Background section at Column 1, line 64 to Column 2, line 8 and in the description of Figure 3B at Column 7, lines 12-29. This ALD layer is thus taught as useful in this position (directly over the gate dielectric layer) only for a very select group of metal electrode materials. The Background description particularly mentions copper and tungsten, and a slightly longer but definitive list of metals is listed in the Detailed Description as follows: "121 represents a metal layer (Cu, W, Al, Au, Ag or Pt)." Col. 7, l. 20.

Because Matsuse et al. limits their disclosure of the desirability of an ALD diffusion barrier directly on the gate dielectric to use under particular elemental metal electrode materials, Applicant submits that Matsuse et al. does not provide motivation to use an ALD process for any diffusion barrier over a dielectric. Certainly Bai et al. provides no teaching or motivation to employ ALD for their barrier layer.

As previously noted, ALD is in general a slow process relative to conventional PVD and CVD methods. Accordingly, without a specific motivation to employ ALD processing, the skilled artisan would not be motivated to substitute Bai's deposition process for ALD. Because Matsuse et al. does not provide generally applicable motivation, Applicant submits that there is no teaching or suggestion to combine Bai et al. with Matsuse et al. unless the particular materials of Matsuse et al. are involved.

Because the claims have been amended to list a particular series of materials useful for electrode tuning in the CMOS context, which do not include the metals of Matsuse et al., Applicant respectfully submits that the skilled artisan would have no motivation to combine the references in a manner to render the pending claims obvious.

Note that Applicant's motivation includes both acting as a diffusion barrier and acting as an etch stop for CMOS patterning. For the etch stop function, neither Matsuse nor Bai et al. give any motivation to use ALD. It is only as a diffusion barrier for Matsuse's limited list of gate electrode materials (Cu, W, Al, Au, Ag, Pt) that their ALD barrier is suggested.

CONCLUSIONS

In view of the following amendments and remarks, Applicant respectfully submits that the application is in condition for allowance and requests the same. If, however, some issue remains that the Examiner feels can be addressed by Examiner's Amendment, the Examiner is cordially invited to call the undersigned for authorization.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: November 23, 2005

By: _____

Adeel S. Akhtar
Registration No. 41,394
Attorney of Record
Customer No. 20,995
(415) 954-4114

2073483
112305